WHAT IS CLAIMED IS:

1. An integrated circuit suitable for connecting to a shared communication bus, comprising:

means for receiving a set of data signals, including first and second data signals, from the shared bus;

a skew compensation circuit including a set of data delay blocks configured to selectively delay each of the set of data signals to produce a set of edge aligned data signals; and

wherein the skew compensation circuit includes a first set of data delay blocks and means for selecting the first set of delay blocks when a first device connected to the shared bus is a sender of data and second delay block and means for selecting the second delay block when a second device connected to the shared bus is the sender wherein the selective delay inserted by the skew compensation varies depending upon the sender of data.

2. The integrated circuit of claim 1, wherein each of the data delay blocks includes a counter configured to increment if a corresponding data signal transitions before a clock signal and further wherein the output of the counter controls the amount of delay inserted into the corresponding data signal.

3. The integrated circuit of claim 2, wherein each data delay block further includes a set of delay buffers connected in series to a data signal and means for selecting one of the delay buffer outputs as the delay block output based on the value of the counter.

4. The integrated circuit of claim 3, wherein each delay buffer output provides an input to a multiplexer and wherein the output of the counter provides the select input to the multiplexer.

5. The integrated circuit of claim 1, wherein the skew compensation circuit further includes first and second clock delay blocks and means for selecting the first or second delay blocks depending on the identity of the sender, wherein each clock delay block is configured to insert

delay into the signal path of a clock signal to produce a clock signal edge aligned with the edge aligned data signals.

6. The integrated circuit of claim 5, further comprising a clock latching edge generator to receive the edge aligned clock signal and produce a clocking signal that is delayed relative to the edge aligned data signals.

7. The integrated circuit of claim 6, wherein the clocking signal is delayed a quarter cycle relative to the edge aligned data signals.

8. A data processing system, comprising:

first, second, and third agents connected via a shared bus;

wherein the third agent is configured to receive information via the shared bus from the first agent and from the second agent;

wherein the third agent includes a skew compensation circuit to determine signal skew associated with signals received via the shared bus and to compensate for the determined skew by adding appropriate delay into selected signals of the bus; and

wherein the skew compensation circuit is enabled to identify the first agent or the second agent as the sender of information received by the third agent via the shared bus and wherein the skew compensation circuit is further enabled to alter the skew compensation based on the identity of the sender wherein the added delay is specific to the corresponding sender.

9. The system of claim 8, wherein the skew compensation circuit includes a set of data delay blocks configured to selectively delay each of the set of data signals to produce a set of edge aligned data signals.

10. The system of claim 9, wherein the skew compensation circuit further includes a first set of data delay blocks and means for selecting the first set of delay blocks when a first device connected to the shared bus is a sender of data and second delay block and means for selecting the second delay block when a second device connected to the shared bus is the sender wherein the selective delay inserted by the skew compensation varies depending upon the sender of data.

11. The system of claim 9, wherein each of the data delay blocks includes a counter configured to increment if the corresponding data signal transitions before a clock signal and further wherein the output of the counter controls the amount of delay inserted into the corresponding data signal.

12. The system of claim 11, wherein each data delay block further includes a set of delay buffers connected in series to a data signal and means for selecting one of the delay buffer outputs as the delay block output based on the value of the counter.

13. The system of claim 12, wherein each delay buffer output provides an input to a multiplexer and wherein the output of the counter provides the select input to the multiplexer.

14. The system of claim 9, wherein the skew compensation circuit further includes first and second clock delay blocks and means for selecting the first or second delay blocks depending on the identity of the sender, wherein each clock delay block is configured to insert delay into the signal path of a clock signal to produce a clock signal edge aligned with the edge aligned data signals.

15. The system of claim 14, further comprising a clock latching edge generator to receive the edge aligned clock signal and produce a clocking signal that is delayed relative to the edge aligned data signals by a quarter cycle.

16. A skew compensation circuit, comprising:

a first set of data delay blocks including a data delay block corresponding to each of a set of data signals of a shared communication bus to which the circuit is coupled;

a second set of data delay blocks including a data delay block corresponding to each of the set of data signals;

wherein each data delay block is configured to insert a variable amount of time delay into the signal path of the delay block's corresponding data signal; and

multiplexers configured to select between the first and second set of data delay blocks.

17. The circuit of claim 16, further comprising a first and a second clock delay block, each configured to receive a clock signal and wherein each data delay block is configured to insert a variable amount of time delay into the signal path of the delay block's corresponding data signal.

18. The circuit of claim 17, wherein the data delay blocks and the clock delay blocks insert delay into their corresponding signals to produce a set of edge aligned data signals and an edge aligned clock signal.

19. The circuit of claim 18, further comprising a clock edge generator circuit to produce a clocking signal delayed one quarter cycle from the edge aligned clock signal and wherein the edge aligned data signals provide inputs to respective latches and wherein each of the respective latches is clocked by the clocking signal.

20. The circuit of claim 16, wherein each of the data delay blocks includes a counter configured to increment if a corresponding data signal transitions before a clock signal and further wherein the output of the counter controls the amount of delay inserted into the corresponding data signal.